Rev. E

LVDS
SR-A2D20 Series

Description

The **SR-A2D20 Series** of quartz crystal oscillators provide LVDS compatible signals in a ceramic SMD package. Systems designers may now specify space-saving, cost-effective packaged LVDS oscillators to meet their timing requirements.

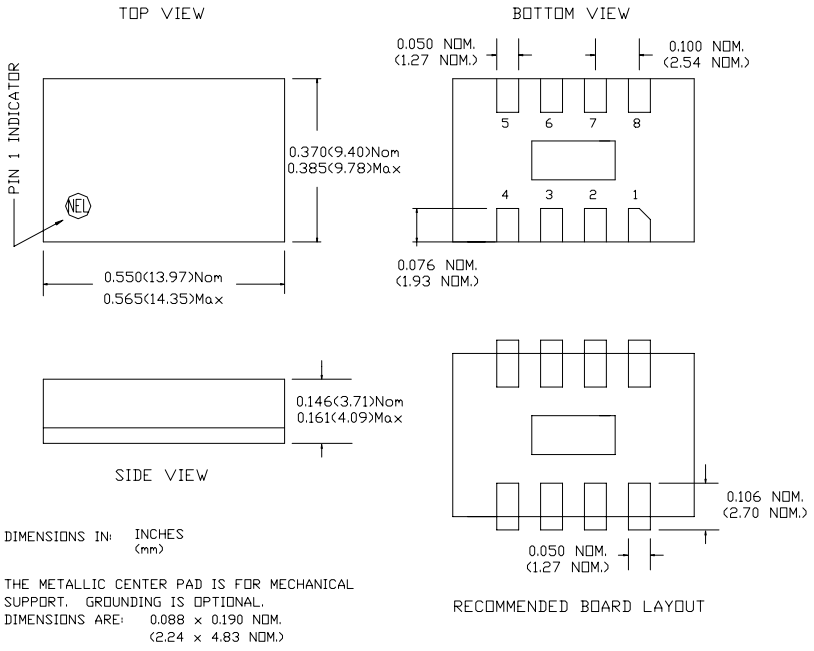
Features

- Wide frequency range–100.0MHz to 640.0MHz
- User specified tolerance available
- Space-saving alternative to discrete component oscillators
- High shock resistance, to 1000g
- 3.3 volt operation (other voltages available upon request)
- Metal lid electrically connected to ground to reduce EMI
- Enable/Disable
- LVDS output on pin 4, complement on Pin 5
- COTS/Dual use
- Low Jitter - Wavecrest jitter characterization available
- High Reliability - NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Overtone technology
- High Q Crystal actively tuned oscillator circuit
- Power supply decoupling internal
- No internal PLL avoids cascading PLL problems
- High frequencies due to proprietary design
- Gold plated pads
- RoHS Compliant, Lead Free Construction

Electrical Connection

Pin	Connection
1	Vcc
2	Ground
3	NC or Ground
4	Q Output
5	/Q Output
6	Ground
7	Ground
8	Enable

NEL recommends connecting the large pad located between the general signal pads to ground for heat transfer and improved RF grounding.



NEL FREQUENCY CONTROLS, INC.
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SR-A2D20 Series Continued
LVDS

Rev. E

Operating Conditions and Output Characteristics (6)

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Frequency	-----	-----	100.0MHz	-----	640.0MHz
Duty Cycle(2)	-----	@ V_O /2	45/55%	-----	55/45%
Logic 0 (2)	V_{OL}	-----	0.80V	-----	1.10V
Logic 1 (2)	V_{OH}	-----	1.25V	-----	1.55V
Differential Voltage (2)	V_{OD}	-----	250 mV	-----	450 mV
Enable Voltage	-----	V_{EE}=0V	-----	-----	0.8V
Disable Voltage(5) -----		V_{EE}=0V 2.0V	-----	-----	
Rise & Fall Time (2)	tr,tf	20-80%V_O	-----	-----	600 ps
Jitter, RMS(3)	-----	-----	-----	-----	1 psec
Frequency Stability (1)	dF/F	Overall conditions including: voltage, calibration, temp., 10 yr aging, shock, vibration	-100ppm	-----	+100ppm
Phase Noise(4)	-----	@100Hz	-----	-----	-80 dBc/Hz
	-----	@1kHz	-----	-----	-115 dBc/Hz
	-----	@10kHz	-----	-----	-130 dBc/Hz
	-----	@100kHz	-----	-----	-130 dBc/Hz
	-----	@1MHz	-----	-----	-135 dBc/Hz
	-----	@10MHz	-----	-----	-135 dBc/Hz

General Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Supply Voltage	V_{CC}	3.3V±5%	3.135V	3.3V	3.465V
Supply Current	I_{CC}	-----	0.0 mA	-----	80 mA
Output current	I_O	Continuous Output Current	0.0 mA	-----	±50.0 mA
Operating temperature	T_A	------	0°C	-----	70°C
Storage temperature	T_S	-----	-55°C	-----	125°C
Power Dissipation	P_D	-----	-----	-----	277 mW
Load	100 ohms across differential outputs				
Start-up time	t_S	-----	-----	2 ms	10 ms

Environmental and Mechanical Characteristics

Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A
Vibration	0.060" double amplitude 10 Hz to 55 Hz, 35g's 55Hz to 2000 Hz

Footnotes:

1) Standard frequency stability (others available)
2) With Load of 100 ohms across differential outputs.
3) Jitter performance is frequency dependent. Please contact factory for full Wavecrest characterization. RMS jitter bandwidth of 12kHz to 20MHz.
4) Phase noise characterization available. Phase Noise is frequency dependant, phase noise specification references a 1.0GHz part.
5) Open to enable pin also enables the output.
6) All parameters, unless otherwise specified, are at nominal conditions, ie: T=25°C, Nominal Vcc & Nominal Load.

Creating a Part Number

SR - A2D2X - FREQ

Package Code
SR 8 pad 9x14 SMD

Input Voltage

Code	Specification
A	3.3V
B	2.5V

Tolerance/Performance

0	±100ppm 0-70°C
1	±50ppm 0-70°C
7	±25ppm 0-70°C
9	Customer Specific
A	±20ppm 0-70°C
B	±50ppm -40 to +85°C
C	±100ppm -40 to +85°C

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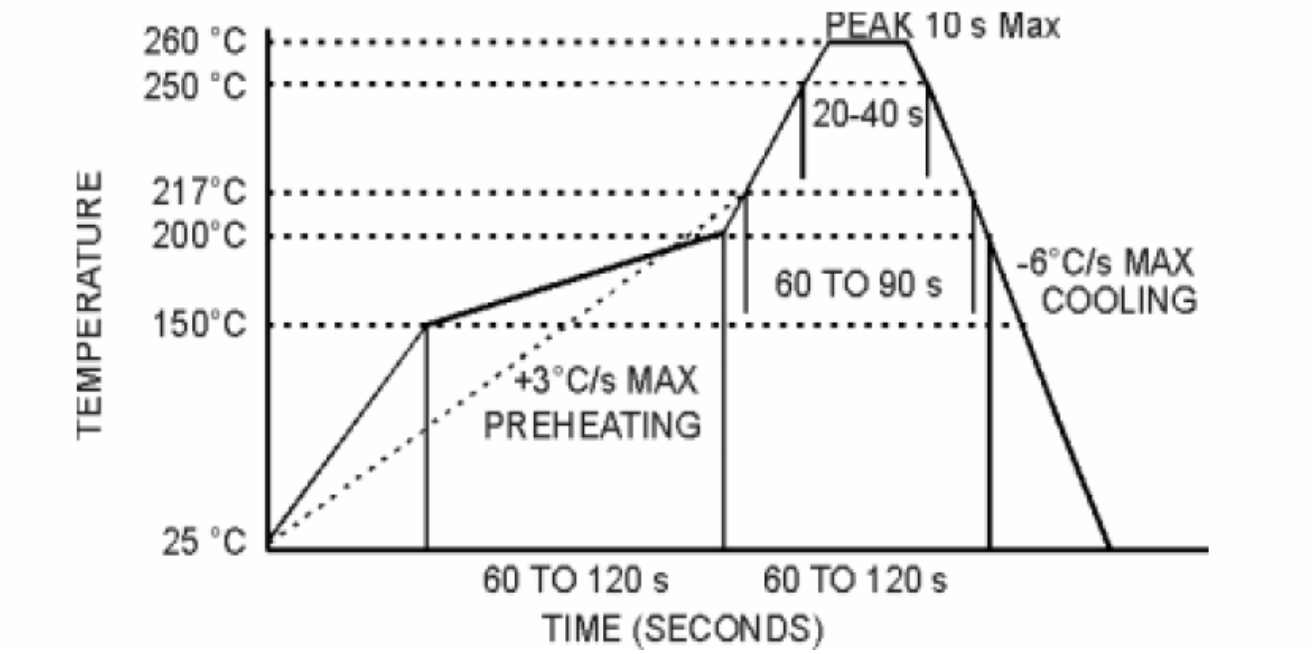
SR-A2D20 Series Continued

Max Reflow Profile



The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended.

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