

O-CCPC0-X-YY-X -10.000 MHz
Phase-Locked SC-cut Clean-up OCXO in Europack

Product Data Sheet

Features

- SC-cut crystal
- Low Phase Noise
- Very Compact Package
- In Absence of REF IN Frequency Returns to Preset Value

Applications

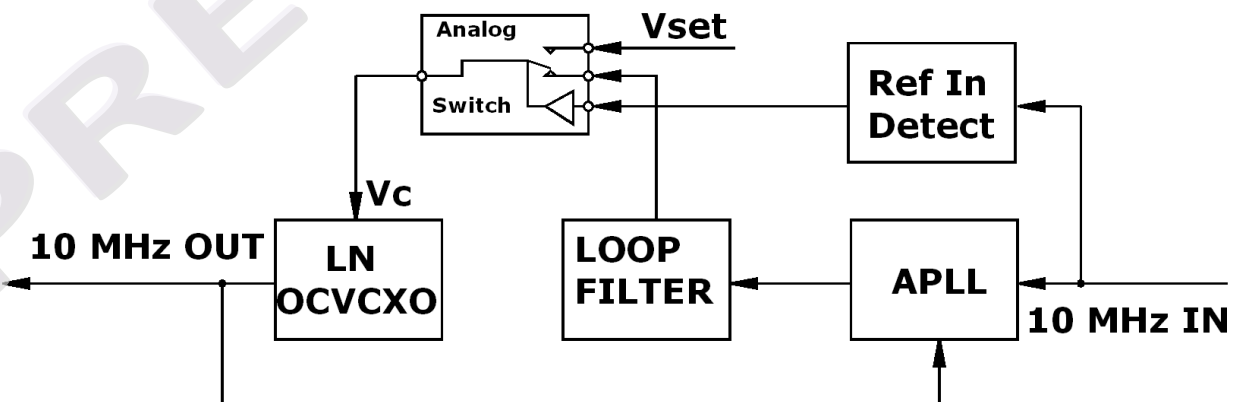
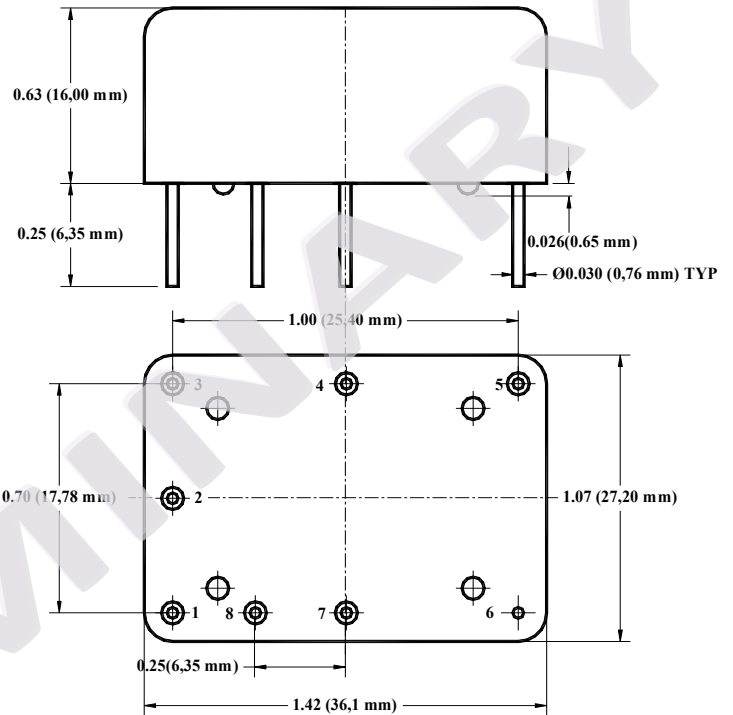
- Significantly improves Phase Noise of incoming signal
- COTS/Dual use

Pinout

Pin #1 - 10 MHz Input; Pin #2 - Vref; Pin #3 - Vcc

Pin #4 - Lock Detect; Pin #5 - RF OUT; Pin #6 - Case, GND

Pin #7 - Input Signal Detect; Pin #8 - Vset.



Specifications:

Rev.

Parameter	Symb	Condition	Min	Typ	Max	Unit	Note
<i>Absolute Maximum Ratings</i>							
Input Break Down Voltage	V _{cc}		-0.5		5.5	V	V _{cc} = 5 V
Operating Temp.	T _o		0		70	°C	
Operable Temp.	T _O		-40		85	°C	
Storage temper.	T _s		-40		85	°C	

Electrical (3)

Input Frequency	F _{in}			10.000		MHz		
Output Frequency	F _{out}			10.000		MHz		
Frequency Capture Range (APR)	ΔF/F	Over All	±100			ppb	When input signal disappears free run within 50 ppb of 10 MHz as shipped, 200 ppb over 10 years	
Allan Deviation		.01s to 0.1s		5E-12				
Frequency stability	ΔF/F	Locked	Equal to incoming signal					
Recommended Input SSB Phase Noise	£(Δf)	10 Hz 100 Hz 1 KHz 10 KHz 100 KHz			-80 -110 -130 -140 -140	dBc/Hz		
Input signal		CMOS Sine Wave	2 0		15	V dBm	swing	
Output SSB Phase Noise Floor	£(Δf)	10 Hz 100 Hz 1 KHz 10 KHz 100 KHz			-125 -145 -162 -165 -169	dBc/Hz	Grade "C"	
Output SSB Phase Noise Floor		10 Hz 100 Hz 1 KHz 10 KHz 100 KHz			-145 -157 -165 -168 -172	dBc/Hz	Grade "U"	
Output SSB Phase Noise Improvement Compared to Input Phase Noise		10 Hz 100 Hz 1 KHz 10 KHz 100 KHz		45 50 50 50 50		dBc/Hz	Cannot improve beyond the noise floor for each grade as listed above	
G-sensitivity		worst direction			±1.0	ppb/G		
Input Voltage	V _{cc}	Code 0	4.75	5.0	5.25	V		
Power consumption	P	steady state, 25°C start-up @ -30°C		1.2 2.8	1.5 3.5	W	Standard Operating Temperature, for Op Temp. 85 °C add 20% Still air for all Lower P available, consult Factory	
Spectral Purity		Subharmonics Spurious Harmonics		none -35	-80 -30	dBc	Output Code S	
Load	Internally AC coupled 50 Ohm (Sinewave) 10K Ohm//15pf (CMOS/TTL)							
Warm-up time	τ	to lock on 100 ppb input		3	5	minutes		



Lock Time after warm-up				1		minute	
Output Power	Pout	Into 50 Ohm	10	13			Output Code S
Logic 1 (CMOS)	Voh		0.7Vref			V	Output Code T
Logic 0 (CMOS)	Vol					0.1Vref	Output Code T
Duty Cycle			45/55			55/45	%
Rise/Fall Time	Tr/Tf			3	5		ns
Preset Voltage	Vset			2.25			V
							Can be externally adjusted by LN Potentiometer 10 KOhm between Vref and GND
Lock Detect				Logic "1"			Can drive LED
Input Detect				Logic "1"			Can drive LED

Environmental and Mechanical

Operating temp. range	0°C to 70°C Standard, Other options – see chart below
Mechanical Shock	Per MIL-STD-202, 30G, 11ms , survival
Vibration	Per MIL-STD-202, 5G to 2000 Hz, Survival

Electrical Connections

Notes:

All parameters, unless otherwise specified, are at nominal conditions, ie: T=25°C, Nominal Vcc & Nominal Load.

Creating a Part Number

0 - **C** **E8** **C** **0** **X** **YY** - **X** **10.000**
MHz
OCXO

Conventional Power
 Package Code
 Europack, 8pin

Phase Noise Grade

Code	Specification
C	Standard
U	Ultimate

Environmental

Code	Specification
L	Contains a level of lead that is in excess of RoHS directive and is not designed for reflow
R	RoHS compliant, not designed for reflow

Supply Voltage

Code	Specification
0	5 V TYP

Output

Code	Specification
S	Sinewave
T	CMOS/TTL

Temperature Range

Code	In 5°C steps **
First letter	Lowest temperature from A = -40°C
Second letter	Highest temperature to Z = 85°C
Examples	
IS	0°C to 50°C
GU	-10°C to 60°C
EW	-20°C to 70°C



****Temperature Code Table**

Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C
A	-40	F	-15	K	10	P	35	U	60	Z	85
B	-35	G	-10	L	15	Q	40	V	65		
C	-30	H	-5	M	20	R	45	W	70		
D	-25	I	0	N	25	S	50	X	75		
E	-20	J	5	O	30	T	55	Y	80		

