



### CMOS HS-1420 Series

### Description

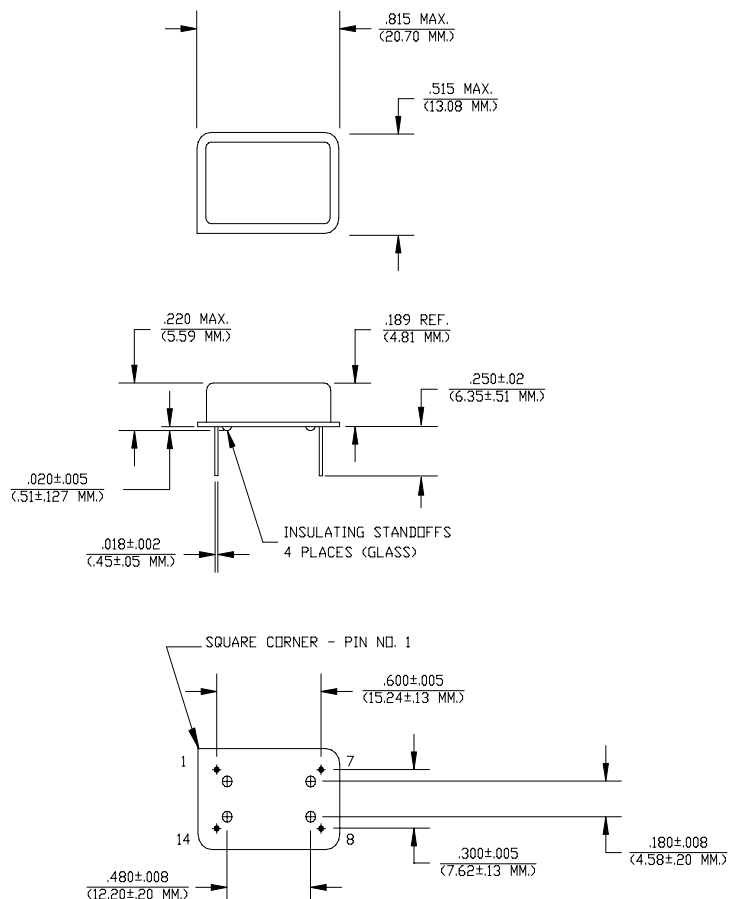
The **HS-1420 Series** of quartz crystal oscillators provide enable/disable 3-state CMOS compatible signals for bus connected systems. Supplying Pin 1 of the HS-1420 units with a logic "1" or open enables its output. In the disabled mode, output pin presents a high impedance to the load. All units are resistance welded in an all metal package, offering RFI shielding, and are designed to survive standard wave soldering operations without damage. Insulated standoffs to enhance board cleaning are standard.

### Features

- Wide frequency range— 0.5MHz to 85MHz
- User specified tolerance available
- Will withstand vapor phase temperatures of 253°C for 4 minutes maximum
- Space-saving alternative to discrete component oscillators
- High shock resistance, to 3000g
- All metal, resistance weld, hermetically sealed package
- Low Jitter
- High Q Crystal actively tuned oscillator circuit
- Power supply decoupling internal
- No internal PLL avoids cascading PLL problems
- Low power consumption
- Gold plated leads - Solder dipped leads available upon request
- RoHS Compliant, Lead Free Construction (unless solder dipped leads are supplied)
- COTS/Dual use

### Electrical Connection

Pin	Connection
1	Enable Input
7	Grd & Case
8	Output
14	V <sub>DD</sub>



Dimensions are in inches and (MM)

HS-1420 Series Continued  
CMOS

Rev. T

### Operating Conditions and Output Characteristics

#### Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Frequency	-----	-----	0.5MHz	-----	85.0MHz
Duty Cycle	-----	@ V <sub>DD</sub> /2	45/55%	-----	55/45%
Logic 0	V <sub>OL</sub>	@ 600µA	-----	-----	0.2V
Logic 1	V <sub>OH</sub>	@ 600µA	V <sub>DD</sub> -0.2V	-----	-----
Rise & Fall Time	tr,tf	10-90% <40MHz	-----	-----	8 ns
		40MHz or greater	-----	-----	6 ns
Tpz	-----	-----	-----	-----	25 ns
Enable/Disable					
Logic High Voltage	-----	-----	3.5V	-----	-----
Enable/Disable					
Logic Low Voltage	-----	-----	-----	-----	1.5V
Jitter, Integrated	J	Integrated from phase noise, 12kHz to 20MHz, RMS	-----	0.1 ps	-----
Jitter, Wavecrest Characterized <sup>(2)</sup>	-----	Random Period	-----	2.3ps	-----
		Accum, pk-to-pk	-----	26ps	-----
Phase Noise	£(Δf)	@ 10Hz	-----	-70 dBc/Hz	-----
		@ 100Hz	-----	-105 dBc/Hz	-----
		@ 1kHz	-----	-130 dBc/Hz	-----
		@ 10kHz	-----	-145 dBc/Hz	-----
		@ 100kHz	-----	-150 dBc/Hz	-----
		@ >1MHz	-----	-150 dBc/Hz	-----
Frequency Stability <sup>(1)</sup>	dF/F	Overall conditions including: voltage, calibration, temp., 10 yr aging, shock, vibration	-100ppm	-----	+100ppm

#### General Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Supply Voltage	V <sub>DD</sub>	-----	4.75V	5.0V	5.25V
Supply Current	I <sub>DD</sub>	No Load	0.0 mA	-----	50mA
Output current	I <sub>O</sub>	-----	0.0 mA	-----	±16.0 mA
Operating temperature	T <sub>A</sub>	-----	0°C	-----	70°C
Storage temperature	T <sub>S</sub>	-----	-55°C	-----	125°C
Power Dissipation	P <sub>D</sub>	-----	-----	-----	263 mW
Lead temperature	T <sub>L</sub>	Soldering, 10 sec.	-----	-----	300°C
Load	-----	-----	-----	-----	15pf
Start-up time	t <sub>s</sub>	-----	-----	2 ms	10 ms

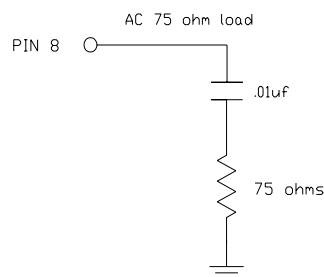
#### Environmental and Mechanical Characteristics

Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A
Vibration	0.060" double amplitude 10 Hz to 55 Hz, 35g's 55Hz to 2000 Hz
Soldering Condition	300°C for 10 seconds
Hermetic Seal	Leak rate less than 1 x 10 <sup>-8</sup> atm.cc/sec of helium

#### Footnotes:

- 1) Standard frequency stability (±20,±25,±50ppm & others available)
- 2) Jitter performance is frequency dependent.  
Please contact factory for full characterization.

#### Test Load:



#### Creating a Part Number

**HS - A142X - FREQ**

Package Code	Tolerance/Performance
HS Leaded 4 pin (14 pin)	0 ±100ppm 0-70°C
SM Leaded 4 pin (14 pin) SMD	1 ±50ppm 0-70°C
Gull Wing	7 ±25ppm 0-70°C
<b>Input Voltage</b>	9 Customer Specific
Code Specification	A ±20ppm 0-70°C
A 3.3V	B ±50ppm -40 to +85°C
5V	C ±100ppm -40 to +85°C



**FREQUENCY  
CONTROLS, INC.**