

**AB-X32AXXX-X Series
CMOS/LVCMOS HF VCXO**

Rev. S

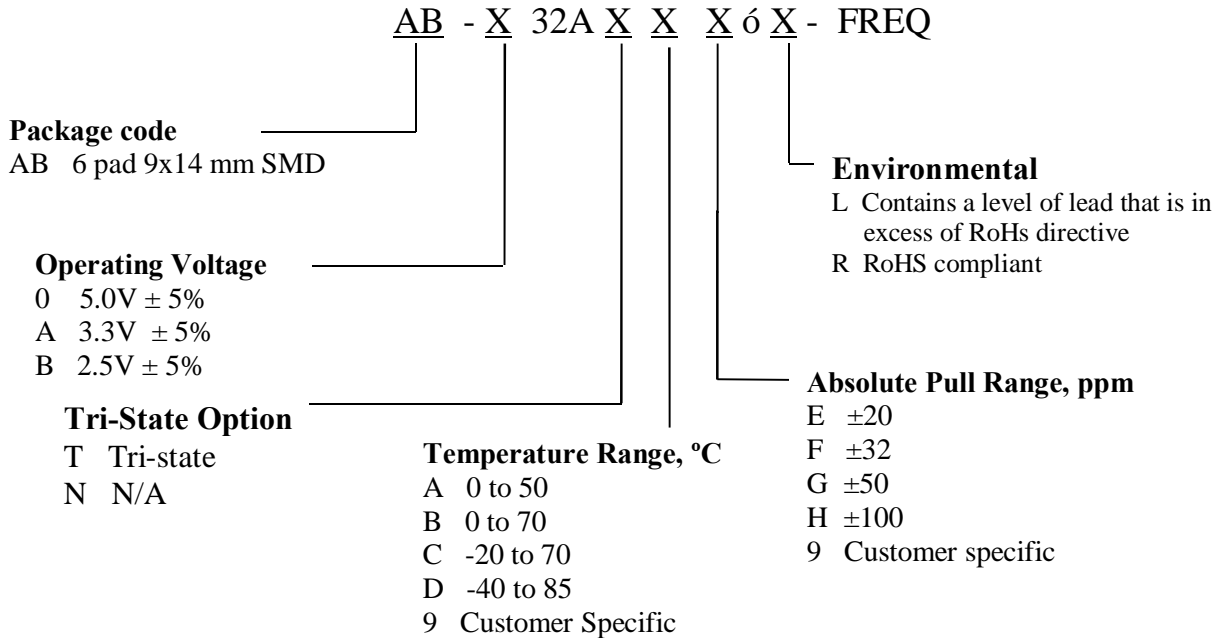
Description

The **AB-X32AXXX Series** of voltage controlled crystal oscillators (VCXO) provides high frequency with CMOS/LVCMOS outputs. The outputs can be Tri-stated for test automation or combining multiple clocks. The device does not use any frequency multiplication, providing exceptionally low Phase Noise and Jitter and wide pull. It's packaged in a miniature, FR-4 based 9x14 mm SMD package

Applications and Features

- Wide frequency range ó 12.0MHz to 250.000MHz
- Fiber Channel; 10 GbE; Infiniband; Network Processors; SONET/SDH
- High Reliability ó NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Ultra Low Phase Noise and Jitter
- High Shock Resistance, to 1000g
- No Multiplication
- Absolute Pull Range (APR) to ±1000 ppm
- SONET ± 20 ppm overall free-run stability available
- COTS/Dual use

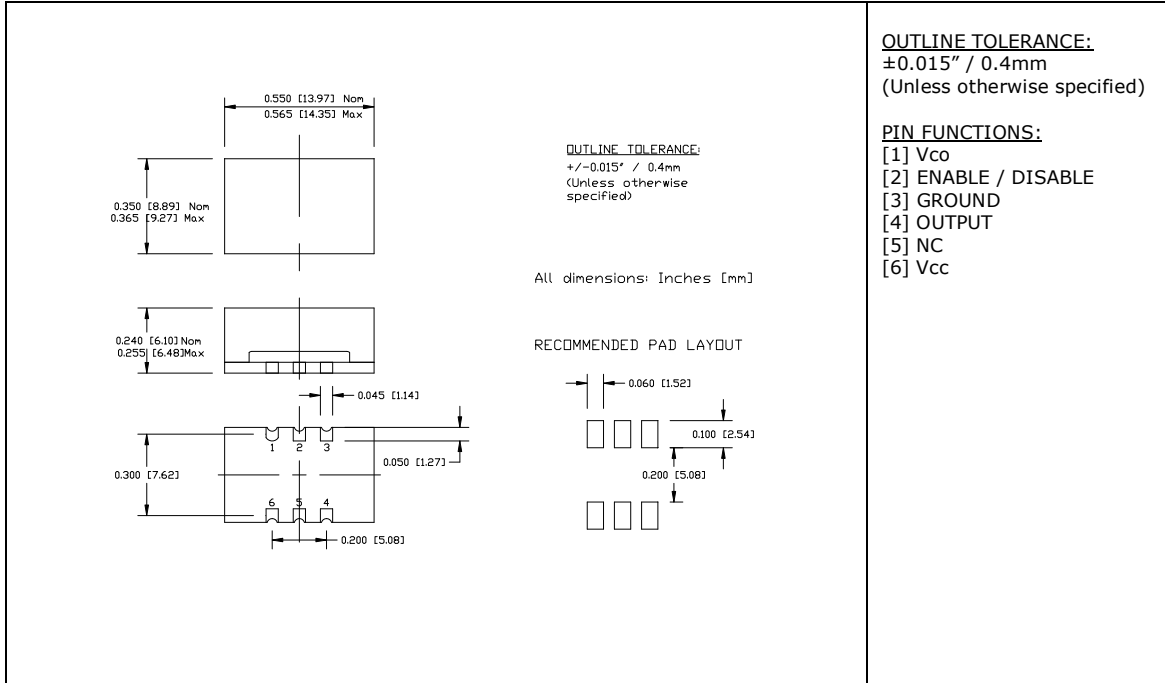
Creating a Part Number



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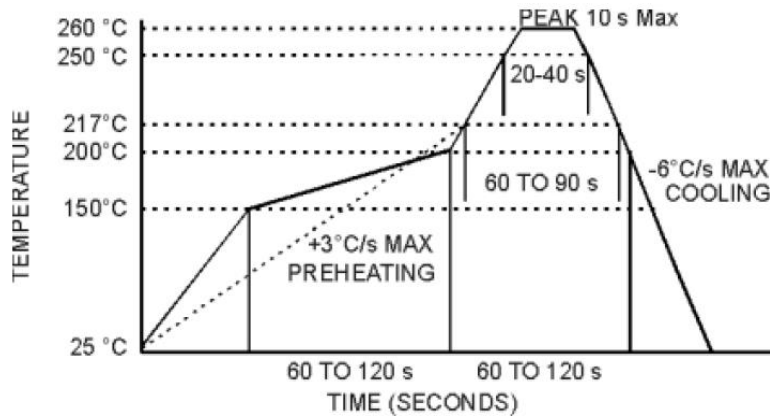
Drawing Specification



Environmental and Mechanical Characteristics

Operating temp. range	see part # table
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. A
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than 1×10^{-8} atm.cc/s of helium
Soldering conditions	See MAX reflow profile below; The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended

MAX Reflow Profile



The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended



**FREQUENCY
CONTROLS, INC.**

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	°C
Storage Temperature Range	Tst	-50 to +90	°C
Supply Voltage	Vcc	-0.5 to 5.5	V
Enable/Disable Voltage	Ven/dis	0 to Vcc	V

Electrical Parameters (1)

Parameter		Symb	Conditions, Note	MIN	TYP	MAX	Unit
Nominal Frequency		Fo		12		250	MHz
Supply Voltage		Vcc	Code 0 Code A Code B	4.75 3.135 2.375	5.0 3.3 2.5	5.25 3.465 2.625	V
Supply current		Icc	No Load, Vcc=3.3V 40MHz			80	mA
Output Logic Type					CMOS		
Load					15pf/10 KOhm		Ohm
Output Levels		Voh Vol	Overall	0.9Vcc		0.1Vcc	V
Duty Cycle(Symmetry)			At 50% Vcc	45/55	50/50	55/45	%
Rise/Fall Time		Tr/Tf	0.2Vcc to 0.8Vcc F<70MHz 70MHz<F<125MHz 125MHz<F<250MHz		3 2 1.5	5 3 2.5	ns
Jitter	Integrated	J	Integrated from Phase Noise, 12 KHz to 20 MHz , RMS		0.1	0.15	ps
			10Hz to 80KHz,RMS			0.8	ps
			50 KHz to 80 MHz		0.2		ps
	Wavecrest characterized		Random period,		2.5		ps
Accumul., pk- to-pk				17		ps	
Deterministic				0		ps	
Phase Noise		£(f)	155.52MHz, APR 50 ppm or less	@ 10 Hz @ 100 Hz @ 1 KHz @ 10KHz @ 100KHz @ >1MHz	-75 -105 -135 -160 -165 -165	-70 -100 -130 -155 -160 -160	dBc/Hz
Sub-harmonics					None		dBc
Frequency Stability usually not specified unless necessary. APR is specified to incorporate stability		F/F	Overall, including temperature, aging 10 years, shock and vibration @ Vc=Vcc/2; APR 50ppm, or less	±20	±30		ppm
Control Voltage Range		Vc		0V		Vcc	V
Setability		Vcs	Vc to set F at Fo; T, Vcc, load ó nominal as shipped	0.4 Vcc	0.5 Vcc	0.6 Vcc	V
Absolute Pull Range		APR	Overall conditions, see part # creation	20,32, 50,100			ppm
Input Impedance		Zin	@ Fmod < 100kHz	50			KOhm
Modulation Bandwidth			At Vc = Vcc/2, -3dB	20			KHz
Enable			Pin 2 = High, or floating	Enabled			V
Disable			Pin 2 = Low	Tri-stted, output ó High Z			V

Note 1. All parameters, unless otherwise specified, are at nominal conditions, ie: T=25°C, Nominal Vcc & Nominal Load.

