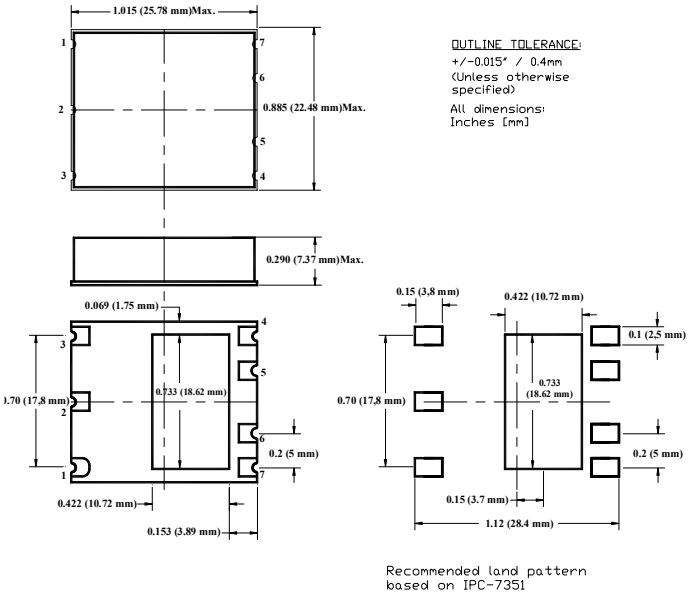
OR-XBFXXXX-X Series
HF/UHF SMD TCVCXO
Ultra Low Phase Noise

Rev. P

Description: The OR-XBFXXXX Series of SMD temperature compensated, voltage-controlled crystal oscillators (TCVCXO), provides High and Ultra High Frequency with excellent temperature stability, ultra low phase noise and jitter with a variety of different output types in a small surface mount FR4-based package.



Features

- **Small, Low Profile SMD Package**
- **Very Low Phase Jitter and Phase Noise**
- **Excellent Frequency Stability**
- **Ultra High Frequency – up to 2.0 GHz**
- **CMOS, Sine-Wave, Differential PECL or LVDS outputs available**
- **Stratum3 available**
- **COTS/Dual use**

  Note: For frequency stability over temperature ±1ppm and tighter, the package height may be 10mm or 12.5mm

NEL recommends connecting the large pad located between the general signal pads to ground for heat transfer and improved RF grounding.

Creating a Part Number

OR - X BF X X X X - X - FREQ

Package Code

OR 7 Pad 25x22x7mm SMD

Supply Voltage

Code	Specification
0	5V ±5%
A	3.3V ±5%

TCXO/TCVCXO Option

Code	Specification
X	No V. Control
V	W/ V. Control

Output Type

Code	Specification
C	CMOS
P	PECL
S	Sine-wave
L	LVDS

Temp. Frequency Stability

Code	Specification
1	±1.0 ppm
2	±2.5 ppm
3	±0.28 ppm
9	Customer Specific

Temperature Range

Code	Specification
E	-10°C to 60°C
B	0°C to 70°C
C	-20°C to 70°C
D	-40°C to 85°C

Environmental

Code	Specification
L	Contains a level of lead that is in excess of RoHS directive.
R	RoHS compliant

Not all combinations available ï consult factory

NEL FREQUENCY CONTROLS, INC.

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Specifications (1)

Parameter	Symb	Condition	Min	Typ	Max	Unit	Note
Electrical							
Frequency Range	F	CMOS LVDS PECL, Sine-wave	30 30 30		200 1,000 2,000	MHz	
Input Voltage	Vcc		3.135 4.75	3.30 5.0	3.465 5.25	V	A 0
Input Current	Icc	CMOS, Sine PECL, Sine, LVDS			30 100 140	mA	@100MHz, 3.3V @622MHz, 3.3V @1000MHz, 3.3V
Frequency Stab.	ΔF/F	Overall, available			±4.6		20 years
Frequency Stability	ΔF/F	vs. Temperature vs. Vcc aging		±0.5 ±0.1 ±1 ±3.5	±1	ppm ppm/V ppm/year ppm	See chart First Year 10 years
Calibration	ΔF/F	As shipped, 25ºC		±0.5	±1	ppm	
Load		CMOS Sine PECL LVDS	15pf/10K Ohm Internally AC-coupled 50 Ohm 50 Ohm to Vcc-2V or Thevenin equivalent 100 Ohm between the outputs receiving end				
Duty cycle		@50%	45	50	55	%	CMOS, PECL, LVDS
Rise/Fall time	Tr/Tf	20 to 80 %		3 0.35		ns	CMOS PECL, LVDS
Logic "1" level	Voh	CMOS	0.9Vcc			V	
Logic "0" level	Vol	CMOS			0.1Vcc	V	
Logic "1" level	Voh	PECL	Vcc-0.96		Vcc-0.81	V	100K available
Logic "0" level	Vol	PECL	Vcc-1.85		Vcc-1.65	V	100K available
Output Levels, LVDS	Vod	Differential Amplitude	247	330	454	mV	
		Amplitude error			50	mV	
	Vof	Offset Voltage	1.125	1.25	1.375	V	
		Offset Voltage Error			50	mV	
Output power (2)	P	Sine-wave Into 50 Ohms </=400MHz	0 4	3 7		dBm	3.3V 5.0V
		>400MHz	-5 0	0 5	5		3.3V 5.0V
Start up time	Ts			2	10	ms	
Phase Jitter		1ů		0.4 0.2	1 0.4	ps	100Hz to 20MHz 12KHz to 20MHz
Subharmonics		PECL, LVDS, Sine PECL, Sine CMOS, Sine		-45 -40	-40 -35 None	dBc	F>250MHz F>1,000MHz F<250MHz
Spurious					-60	dBc	
Harmonics		Sine-wave		-30	-25 -15	dBc	F<1,000MHz F Ć1,000MHz
SSB Phase Noise		@10Hz @100 Hz @1 KHz @10 KHz @100 KHz		-80 -110 -140 -155 -160		dBc/Hz	@100MHz
SSB Phase Noise		@10Hz @100 Hz @1 KHz @10 KHz @100 KHz		-60/-60 -90/-90 -120/-120 -140/-145 -145/-150		dBc/Hz	@622MHz; PECL, LVDS/Sine
SSB Phase Noise		@10Hz @100 Hz @1 KHz @10 KHz @100 KHz		-60 -90 -120 -130 -135		dBc/Hz	@1,000MHz

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Electrical (continued)

Parameter	Symb	Condition	Min	Typ	Max	Unit	Note
Input Impedance			> 10KOhm				
Control voltage	Vc		0		3.3	V	
Modulation bandwidth	MB		2 Hz				Contact Factory for wider MB
Deviation		Vc=0V to 3.3V,25°C	±5	±7		ppm	

Note 1) All parameters, unless otherwise specified, are at nominal conditions, ie: T=25°C, Nominal Vcc & Nominal Load
2) Higher output power available ï consult factory (current consumption may increase)

Absolute Maximum Ratings

Parameter	Symb	Condition	Min	Typ	Max	Unit	Note
Input Break Down Voltage	Vcc		-0.5		5.5	V	
Storage temp.	Ts		-40		105	° C	
Contr. Voltage	Vc		-1		9	V	

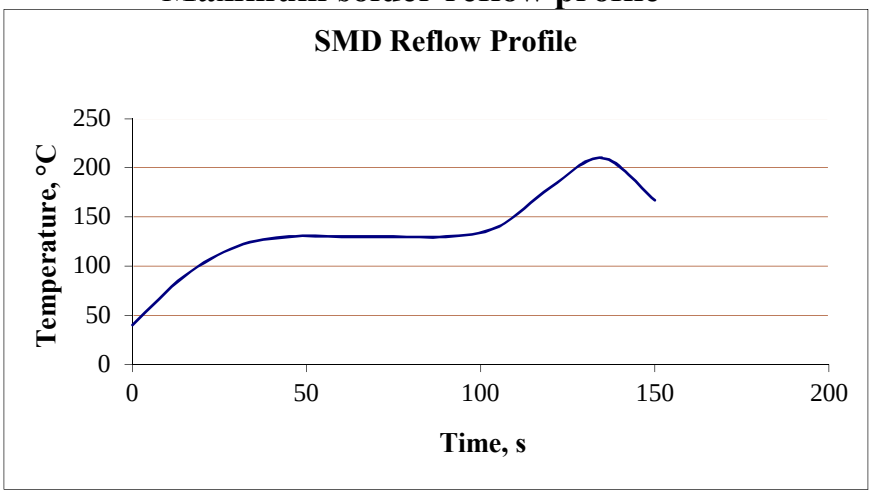
Environmental and Mechanical

Operating temp. range	0°C to 70°C , -40°C to 85°C, see chart, page 1
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. E
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Soldering Conditions	See MAX reflow profile; The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended.
Hermetic Seal	Leak rate less than $1x10^{-8}$ atm.cc/s of helium (crystal only)

Electrical Connections

Pin Out	Pin #1- Voltage Control ; Pin #2 ï N/C ; Pin #3 ï Vcc; Pin#4 ï Output, CMOS, or Sine; Pin #5 ï PECL/LVDS Output; Pin #6 ï PECL/LVDS Complementary Output; Pin #7 - GND

Maximum solder reflow profile



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