

**O-CS8-XXXXXXXX-X**  
**Ultra Low Phase Noise, Precision SC-cut HF**  
**OCXO in 14x21x7.5 mm SMD Package**

Rev. P

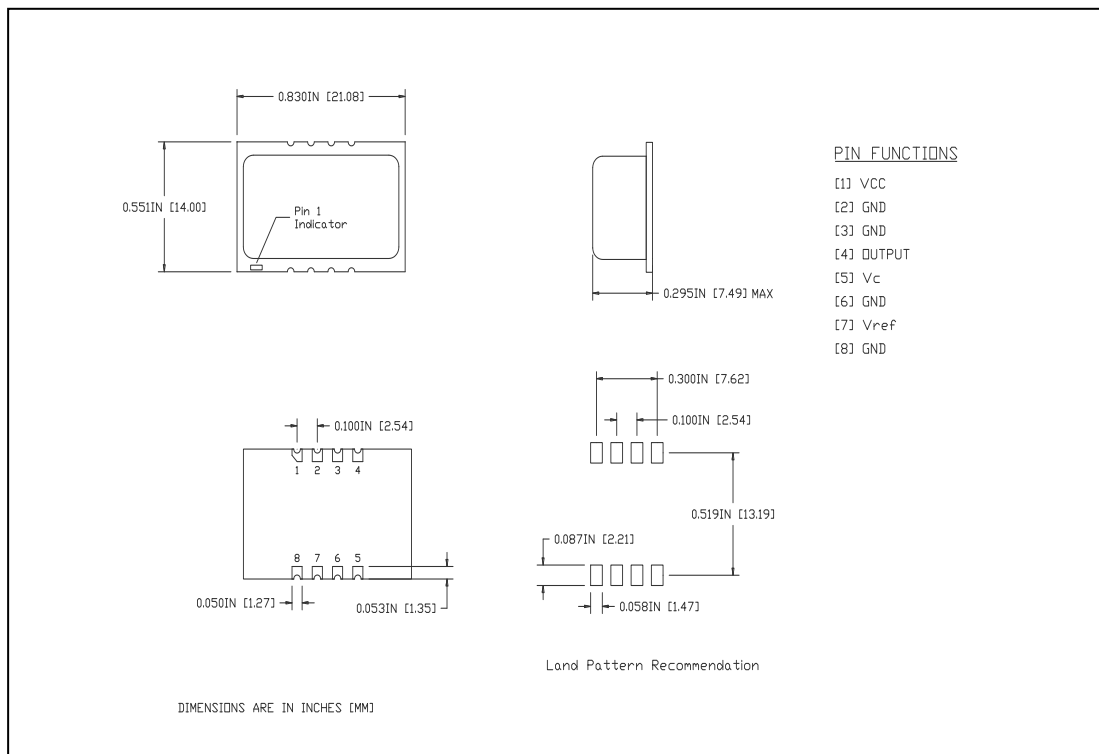
**Product Data Sheet**

**Features**

- SC-cut crystal
- Ultra Low Phase Noise
- Sine Wave +15 dBm output
- Extremely Small, Slim Package

**Applications**

- Instrumentation
- Radar
- High End Synthesizers
- Telecommunication Systems
- Data Communications



# OVEN CONTROLLED CRYSTAL OSCILLATORS

Data Sheet 1319A

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Parameter	Symb	Condition	Min	Typ	Max	Unit	Note		
<b>Absolute Maximum Ratings</b>									
Input Break Down Voltage	V <sub>cc</sub>		-0.5		6.5	V	V <sub>cc</sub> option 0		
Storage temper.	T <sub>s</sub>		-55		85	°C			
Control Voltage	V <sub>c</sub>		-1		10.5	V			
<b>Electrical (1)</b>									
Frequency	F		80		120	MHz			
Frequency stability	ΔF/F	vs. Temp.		±50		ppb	See table below Note 2		
		vs. Supply			2	ppb/5% change			
		Vs. load			2	ppb/5% change			
Aging		per day per first year 10 years		5E-9 5E-7	2.0	ppm	After 30 days of continuous operation		
Allan Deviation		.01s to 1s		5E-11					
SSB Phase Noise at 100.000 MHz	£(Δf)	10 Hz		-95			Grade "L"		
		100 Hz			-125				
		1 KHz			-158				
		10 KHz			-170				
		100 KHz			-178				
		10 Hz			-100			Grade "P"	
		100 Hz				-130			
		1 KHz				-160			
		10 KHz				-172			
		100 KHz				-178			
		10 Hz				-105			Grade "U", Available with slope option "L"
		100 Hz				-135			
1 KHz				-162					
10 KHz				-175					
100 KHz				-180					
Retrace		After 30 minutes		±20		ppb			
G-sensitivity		worst direction			±0.5	ppb/G			
Supply Voltage		5V±5%	4.75	5.0	5.25	V	Option "0" Option A		
		3.3V±5%	3.165	3.30	3.465				
Power consumption	P	steady state, 25°C		1.0	1.2	W	Still air		
		steady state, -40°C start-up		2.5 3.0					
Spectral Purity, Sine wave		Output power	12	15		dBm	Non-supply related		
		Subharmonics		none		dBc			
		Spurious			-80				
		Harmonics		-35	-30				
Output Waveform		Sine		Code S					
		CMOS		Code T					
Load		10KOhm//15pF (HCMOS/TTL), AC-coupled 50 Ohm (Sine-wave)					Output Code T Output Code S		
Warm-up time	τ	to 0.1ppm accuracy		3	5	minutes			
Logic 1 (CMOS)	V <sub>oh</sub>		0.7 V <sub>ref</sub>				Output Code T		
Logic 0 (CMOS)	V <sub>ol</sub>				0.1 V <sub>ref</sub>	V	Output Code T		
Control voltage	V <sub>c</sub>		0		10.0	V	Slope options "L", "M" Slope options "P", "Q" Slope option "K"		
			0		4.5				
			0		3.0				
Input Impedance	Z <sub>in</sub>	At V <sub>c</sub> Pin	10			K ohm			
Pull range		from nominal F		±2.5		ppm			
Absolute pull range	APR		±0.5			ppm			
Deviation slope		Monotonic, posit		0.7		ppm/V	Slope options "L", "M" Slope options "P", "Q"		
				1.3					
Linearity			±10%						
Reference Voltage	V <sub>ref</sub>			N/A		V	Slope options "L", "M" Slope options "P", "Q" V <sub>cc</sub> option A		
				4.5					
				3.0					
Setability	V <sub>c0</sub>	@25°C, F <sub>nom</sub> .	4.0	5.0	6.0	V	Slope options "L", "M" Slope options "P", "Q" Slope option "K"		
			1.75	2.25	2.75				
			1.2	1.5	1.8				
Modulation Bandwidth	F <sub>m</sub>		DC		1	KHz			

All parameters for 100.000 MHz

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**Environmental and Mechanical**

<b>Operating temp. range</b>	0 to 70°C Standard, Other options – see Chart below
<b>Mechanical Shock</b>	Per MIL-STD-202, 30G, 11ms
<b>Thermal Shock</b>	Per MIL-STD-883, Method 1011, Condition A
<b>Vibration</b>	Per MIL-STD-202, 5G to 2000 Hz
<b>Operational vibration</b>	Phase noise under vibration to be verified by the customer
<b>Seal</b>	Only crystal resonator is hermetically sealed
<b>Soldering Conditions</b>	See MAX reflow profile below; The device may be reflowed once. Reflowing upside down is not allowed. Hand soldering is highly encouraged. NO CLEAN assembly is recommended
<b>Moisture Sensitivity</b>	Class 1

**Electrical Connections**

<b>Pin Out</b>	Pin #1-- Vcc; Pins ##2,3,6,8 – GND; Pin #4 – OUTPUT; Pin #5– Vc; Pin #7 - Vref
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**Creating a Part Number**

**O - C S8 - X X X XX XX X - X** - Frequency, MHz

OCXO

Conventional Power

**Package Code**

S8 14x21x7.5 mm SMD

**Supply Voltage**

Code	Specification
0	5.0V ±5%
A	3.3V ±5%

**Control Voltage**

Code	Specification
K	0 to 3.0 V, Internally biased to Vref/2, 100 K Ohm divider
L	0 to 10 V, internally biased to Vref, 100 KOhm
M	0 to 10 V, no internal bias
P	0 to 4.5 V, Internally biased to Vref/2, 100 K Ohm divider
Q	0 to 4.5 V, no internal bias

**Output**

Code	Specification
S	Sinewave
T	CMOS/TTL

**Temperature Stability**

Code	Specification
17	1x10 <sup>-7</sup>
58	5x10 <sup>-8</sup>
YZ	Yx10 <sup>-Z</sup>

**Environmental**

Code	Specification
L	Contains a level of lead that is in excess of RoHS directive and is not designed for reflow
R	RoHS compliant

**Phase Noise Grade (see table)**

Code	Specification
L	Standard
P	Premium
U	Ultimate

**Temperature Range**

Code	In 5°C steps **
First letter	Lowest temperature from A = -40°C
Second letter	Highest temperature to Z = 85°C
Examples	
IS	0°C to 50°C
GU	-10°C to 60°C
EW	-20°C to 70°C

**\*\*Temperature Code Table**

Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C
A	-40	F	-15	K	10	P	35	U	60	Z	85
B	-35	G	-10	L	15	Q	40	V	65		
C	-30	H	-5	M	20	R	45	W	70		
D	-25	I	0	N	25	S	50	X	75		
E	-20	J	5	O	30	T	55	Y	80		



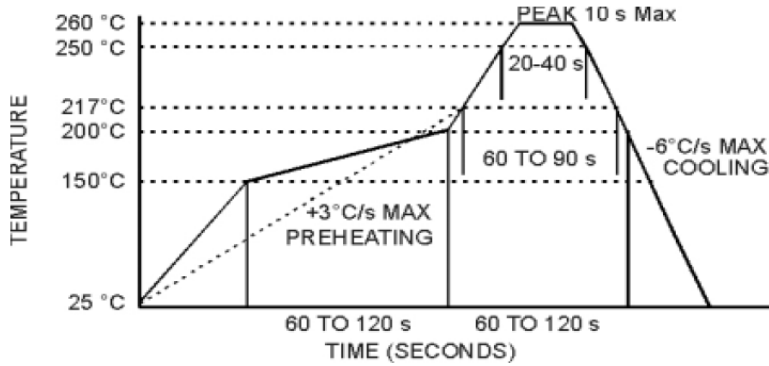
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Notes:

1. Not all combinations are available – consult factory
2. It's not recommended to over-specify stability over temperature performance: it significantly affects the cost.
3. Unless absolutely necessary do not specify highest operating temperature above 70°C
4. All parameters, unless otherwise specified, are at nominal conditions, i.e.: T=25°C, Nominal Vcc & Nominal Load.

**MAX Reflow Profile**



**NOISE XT**

Phase Noise Plot

